Racyics® IP Catalogue 2026

GlobalFoundries® 22FDX®

Racyics provides IP Products for GlobalFoundries 22FDX, enabling ultra-low-power, high-performance system-on-chip (SoC) designs. With a focus on adaptive body biasing (ABB), efficient power management, and robust clock generation, our IP portfolio ensures optimal performance and energy efficiency across a wide range of applications.

	IP	Supply [V]	Key Features	GF 22FDX EXT	GF 22FDX PLUS
ABX	Adaptive Body Bias (ABB) Generator IP for GF 22FDX (ABX®)				
	Both types	Body bias generation: **1.80** Control logic: **0.80**	• Integrated **ABB control loop** • **10 MHz** < fref < **50 MHz** • Area < 0.006 mm² (smallest pump strength) Independent Adaption: • **-0.2 V < VNW < 2.4 V** • **-2.4 V < VPW < 0.2 V**		
	Consumer type only	PVT monitors: 0.40 / 0.45 / 0.50 / 0.55 / 0.60 / 0.65 / 0.80 / 0.90	P_{active} < **12 µW** (typical)	✓	✓
	Automotive type only	PVT monitors: 0.80	• P_{active} < **200 µW** (typical) • **Automotive grade-1 and grade-2** compliant • ISO26262 SEooC with **ASIL D** capability	✓	***

	Standard Cell Libraries with > 300 cells		VT Options	Gate Length		
ABX PLATFORM	8T	0.40 / 0.45 / 0.50 / 0.60 / 0.80 ABB: **forward body bias**	SLVT, LVT	• C20 • C24 • C28 • C32 • C36	✓	*
		0.55 / 0.65 / 0.80 / 0.90 ABB: **reverse body bias**	RVT, HVT		✓	✓**
	9T automotive grade 1	0.80 ABB: **reverse body bias**			✓	✓*
	Characterization corners for - 40 °C to 150 °C temperature range for **Racyics ABX aware timing and power sign-off**					
	Dual-Rail Single Port SRAM (Static Random Access Memory) generator for ULV designs with forward body bias capability	Core logic: 0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 Bitcells: 0.80 ABB: **forward body bias**	• 6t SRAM based on P124 bitcell • Power saving mode: **retention mode** & option to reduce VDD supply during inactivity		✓	*
	Single-Rail Single Port SRAM generator for ULV designs with reverse body bias capability	0.55 / 0.80 ABB: **reverse body bias**	• 6t SRAM based on R188 bitcell • Power saving mode: option to reduce VDD supply during inactivity		✓	*
	Single-Rail Single Port SRAM with Power Down with reverse body bias capability	0.55 / 0.80 ABB: **reverse body bias**	• 6t SRAM based on R188 bitcell • Power saving mode: **retention mode & power down**		✓	*
	Single-Rail Single Port ROM (read-only memory) Macros	0.55 / 0.80 (0.65) ABB: **reverse body bias**	Option to reduce VDD supply during inactivity		✓	*
	Single-Rail Single Port cryo-optimized SRAM with Power Down	0.80 ABB: **forward body bias*** **	• 6t SRAM based on S188 bitcell • **Prototype optimized for Cryo** • Power saving mode: **retention mode & power down**		✓***	*
	Micro Two Port, Dual-Rail, forward-bias SRAM	0.80 ABB: **forward body bias**	**8t SRAM based on R250 bitcell**		✓***	*

* Available for GF 22FDX+ up on request.
✓* Available for specific corner subset.
** Available in Q2/2026.
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*** Currently in development.

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	IP	Supply [V]	Key Features	GF 22FDX EXT	GF 22FDX PLUS
ULP PLATFORM	**Digital Wrapper for Clock and Power Supply IP** for GF 22FDX			✓	*
	Low Power Bandgap Voltage Reference	VDDA18: 1.62 - 1.98 VDD: 0.72 - 0.88	• Two separate output voltages: **400 mV** and **600 mV** with independent trimming, • reference-good detection signal	✓	**
	Nominal **50 MHz Frequency Clock Generator**	0.80 (V_{ref}= 0.60)	• **< 50 ps RMS period jitter** and < 800 ps total jitter (TJ) • < 5 ps / mV supply sensitivity • Power consumption **10 µW** typical and 30 µW maximum	✓	**
	Step-down **DC-to-DC Voltage Converter** (Buck Converter)	VDDA18, VDDP 18: 1.62 - 1.98 VDD: 0.72 - 0.88	• Output voltage **0.4 V - 0.9 V** in steps of 25 mV • can be software-configured on-the-fly • enables Dynamic Voltage and Frequency Scaling **can power ABX domain**	✓	**
	Linear Regulator 1.8 V to core supply	1.80 (V_{ref}= 0.4)	• 1.8 V input to 0.8 V output Output current up to 8 mA • Power good indication • **Disable function** for low power consumption **< 0.5 µW**	✓	**
RACYICS COMPLEMENTARY IP PRODUCTS	General purpose **1.8 V IO Library** with combined GPIO / LVDS, Analog and Special Function IOs	IO: 1.20 / 1.50 / 1.80 core: 0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 (cell-type dependent)	• Supports a wide range of **Metalstack Options** • Various **Pads & Bump** Sizes • approx. 60 IO cells	✓	**
	All-Digital Phase Lock Loop (ADPLL) **2 GHz Clock Generator** based on a Digitally Controlled Oscillator (DCO) with programmable clock frequency dividers	0.80	• 800 MHz ≤ **DCO frequency** ≤ 2400 MHz • **lock-in < 25 µs** • **8-phase** clock output (each 45° phase shift) • Compliant to automotive grade-1 • f_{ref} up to 150 MHz • < 15 ps RMS longterm jitter	✓	*
	ULP All-Digital Frequency Locked Loop (ADFLL) **10 MHz Clock Generator**	0.80	• **10 MHz clock** • **High energy efficiency: 5 µW** during operation • f_{ref}≤ 32 kHz to 1 MHz> • Can be used as clock input for Racyics ABX generator	✓	*
	ULV Integer-N Bang-Bang All-Digital Phase Locked Loop (BB-ADPLL) **1 GHz Clock Generator** In a fully digital architecture	0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80	• **20 MHz up to 1 GHz.** • 100 µW power consumption for a 100 MHz output clock at 0.5 V • Fast lock-in and instant frequency changes • The Racyics ABX enabled implementation reduces jitter at low supply voltages	✓	*
	Voltage and Temperature Sensor with integrated analog-to-digital converter (ADC) and band-gap voltage reference	VDDA: 1.62 to 1.98 VDD: 0.80	• 3 single-ended voltage measurement inputs • **1st order Delta-Sigma ADC** with configurable Oversampling ratio • Resolution up to 12 bit	✓	**
	Crystal oscillator designed to work with 32 kHz crystal	IO: 1.80 core : 0.80	• Bypass & Off mode, • $t_{startup}$ ≈ 58 ms • Compatible with Racyics IO lib	✓	*
	Universal Chiplet Interconnect Express (UCIe) PHY supporting 4 GT/s and 8 GT/s data rates	0.80	• Support for UCIe-S (standard package) • configuration with x16 data width130 µm bump pitch	✓	***

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