

Racyics provides IP Products for GlobalFoundries 22FDX, enabling ultra-low-power, high-performance system-on-chip (SoC) designs. With a focus on adaptive body biasing (ABB), efficient power management, and robust clock generation, our IP portfolio ensures optimal performance and energy efficiency across a wide range of applications.

IP		Supply [V]	Key Features	GF 22FDX	
				EXT	PLUS
ABX	Adaptive Body Bias (ABB) Generator IP for GF 22FDX (ABX®)				
	Both types	Body bias generation: 1.80 Control logic: 0.80	<ul style="list-style-type: none">Integrated ABB control loop10 MHz < fref < 50 MHzArea < 0.006 mm² (smallest pump strength)Independent Adaption:<ul style="list-style-type: none">-0.2 V < VNW < 2.4 V-2.4 V < VPW < 0.2 V		
	Consumer type only	PVT monitors: 0.40 / 0.45 / 0.50 / 0.55 / 0.60 / 0.65 / 0.80 / 0.90	P _{active} < 12 μW (typical)	✓	✓
	Automotive type only	PVT monitors: 0.80	<ul style="list-style-type: none">P_{active} < 200 μW (typical)Automotive grade-1 and grade-2 compliantISO26262 SEooC with ASIL D capability	✓	✓**

ABX PLATFORM	Standard Cell Libraries with > 300 cells		VT Options	Gate Length		
	8T	0.40 / 0.45 / 0.50 / 0.60 / 0.80 ABB: forward body bias	SLVT, LVT	<ul style="list-style-type: none">C20C24C28C32C36	✓	*
		0.55 / 0.65 / 0.80 / 0.90 ABB: reverse body bias	RVT, HVT		✓	✓*
	9T automotive grade 1	0.80 ABB: reverse body bias			✓	✓*
	Characterization corners for - 40 °C to 150 °C temperature range for Racyics ABX aware timing and power sign-off					
	Dual-Rail Single Port SRAM (Static Random Access Memory) generator for ULV designs with forward body bias capability	Core logic: 0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 Bitcells: 0.80 ABB: forward body bias	<ul style="list-style-type: none">6t SRAM based on P124 bitcellPower saving mode: retention mode & option to reduce VDD supply during inactivity	✓	*	
	Single-Rail Single Port SRAM generator for ULV designs with reverse body bias capability	0.55 / 0.80 ABB: reverse body bias	<ul style="list-style-type: none">6t SRAM based on R188 bitcellPower saving mode: option to reduce VDD supply during inactivity	✓	✓	
	Single-Rail Single Port SRAM with Power Down with reverse body bias capability	0.55 / 0.80 ABB: reverse body bias	<ul style="list-style-type: none">6t SRAM based on R188 bitcellPower saving mode: retention mode & power down	✓	✓	
	Single-Rail Single Port ROM (read-only memory) Macros	0.55 / 0.80 (0.65) ABB: reverse body bias	Option to reduce VDD supply during inactivity	✓	**	
	Single-Rail Single Port cryo-optimized SRAM with Power Down	0.80 ABB: forward body bias	<ul style="list-style-type: none">6t SRAM based on S188 bitcellPrototype optimized for CryoPower saving mode: retention mode & power down	✓	*	
	Micro Two Port, Single-Rail, forward-bias SRAM	0.80 ABB: forward body bias	8t SRAM based on R250 bitcell	***	***	

* Available for GF 22FDX+ up on request.
✓* Available for specific corner subset.

** Available in Q1/2027. *** Currently in development.
✓** Available for PLUS-AP150 PDK.

IP		Supply [V]	Key Features	GF 22FDX	
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ULP PLATFORM	Digital Wrapper for Clock and Power Supply IP for GF 22FDX				
	Low Power Bandgap Voltage Reference	VDDA18: 1.62 - 1.98 VDD: 0.72 - 0.88	<ul style="list-style-type: none">Two separate output voltages: 400 mV and 600 mV with independent trimmingreference-good detection signal	✓	✓
	Nominal 50 MHz Frequency Clock Generator	0.80 (V _{ref} = 0.60)	<ul style="list-style-type: none">< 50 ps RMS period jitter and < 800 ps total jitter (TJ)< 5 ps / mV supply sensitivityPower consumption 10 μW typical and 30 μW maximum	✓	✓
	Step-down DC-to-DC Voltage Converter (Buck Converter)	VDDA18, VDDP 18: 1.62 - 1.98 VDD: 0.72 - 0.88	<ul style="list-style-type: none">Output voltage 0.4 V - 0.9 V in steps of 25 mVcan be software-configured on-the-flyenables Dynamic Voltage and Frequency Scalingcan power ABX domain	✓	✓
	Linear Regulator 1.8 V to core supply	1.80 (V _{ref} = 0.4)	<ul style="list-style-type: none">1.8 V input to 0.8 V outputOutput current up to 8 mAPower good indicationDisable function for low power consumption < 0.5 μW	✓	✓
RACYICS COMPLEMENTARY IP PRODUCTS	General purpose 1.8 V IO Library with combined GPIO / LVDS, Analog and Special Function IOs	IO: 1.20 / 1.50 / 1.80 core: 0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 (cell-type dependent)	<ul style="list-style-type: none">Supports a wide range of Metalstack OptionsVarious Pads & Bump Sizesapprox. 60 IO cells	✓	✓
	All-Digital Phase Lock Loop (ADPLL) 2 GHz Clock Generator based on a Digitally Controlled Oscillator (DCO) with programmable clock frequency dividers	0.80	<ul style="list-style-type: none">800 MHz ≤ DCO frequency ≤ 2400 MHzlock-in < 25 μs8-phase clock output (each 45° phase shift)Compliant to automotive grade-1f_{ref} up to 150 MHz< 15 ps RMS longterm jitter	✓	✓
	ULP All-Digital Frequency Locked Loop (ADFLL) 10 MHz Clock Generator	0.80	<ul style="list-style-type: none">10 MHz clockHigh energy efficiency: 5 μW during operationf_{ref}≤ 32 kHz to 1 MHz>Can be used as clock input for Racyics ABX generator	✓	✓
	ULV Integer-N Bang-Bang All-Digital Phase Locked Loop (BB-ADPLL) 1 GHz Clock Generator In a fully digital architecture	0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80	<ul style="list-style-type: none">20 MHz up to 1 GHz100 μW power consumption for a 100 MHz output clock at 0.5 VFast lock-in and instant frequency changesThe Racyics ABX enabled implementation reduces jitter at low supply voltages	✓	✓
	Voltage and Temperature Sensor with integrated analog-to-digital converter (ADC) and band-gap voltage reference	VDDA: 1.62 to 1.98 VDD: 0.80	<ul style="list-style-type: none">3 single-ended voltage measurement inputs1st order Delta-Sigma ADC with configurable Oversampling ratioResolution up to 12 bit	✓	✓
	Crystal oscillator designed to work with 32 kHz crystal	IO: 1.80 core : 0.80	<ul style="list-style-type: none">Bypass & Off modet_{startup} ≈ 58 msCompatible with Racyics IO lib	✓	✓
	Universal Chiplet Interconnect Express (UCIe) PHY supporting 4 GT/s and 8 GT/s data rates	0.80	<ul style="list-style-type: none">Support for UCIe-S (standard package)configuration with x16 data width, 130 μm bump pitch		✓**

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