Racyics® Single Rail SRAM

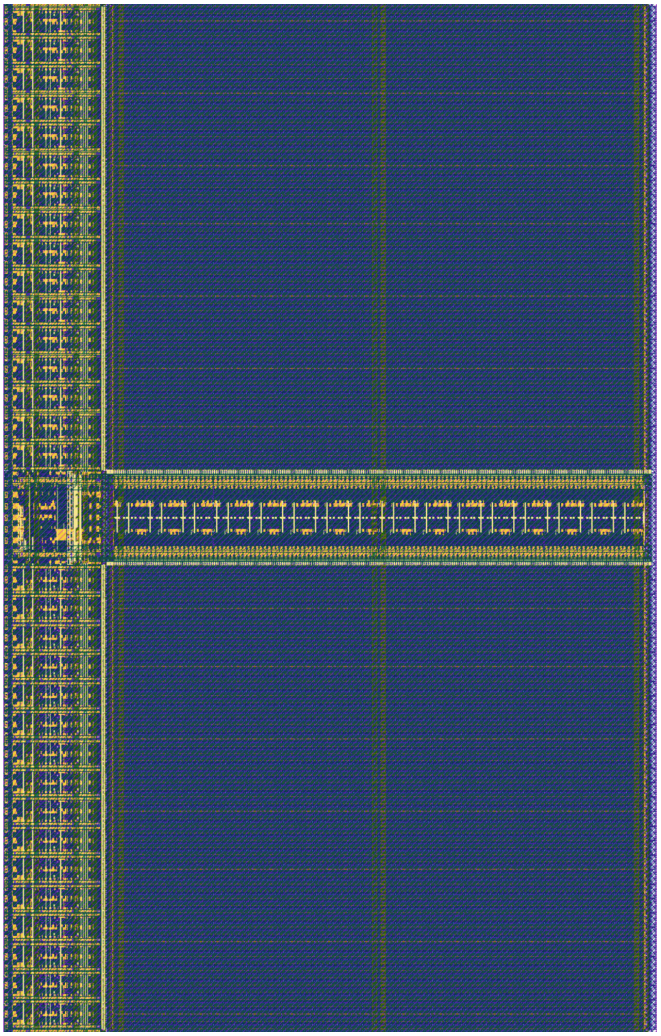
GlobalFoundries® 22FDX®

DESCRIPTION

Ultra-low voltage logic designs using adaptive body biasing demand dense SRAM solutions which fully integrate in the ABB aware implementation and sign-off flow of the **Racyics ABX® Platform** solution. The Racyics Single Rail SRAM supports ultra-low voltage operation down to **0.55 V** where logic designs with **Minimum-Energy-Point** are implemented.

KEY FACTS

- Single port SRAM compiler based on Racyics R188 logic memory cell with dual-well architecture
- Supply voltage 0.55 V to 0.8 V enabled with Racyics ABX
- Direct interfacing to ULV Racyics ABX digital standard cell domains without additional level shifters
- Full set of characterization corners for -40 °C to 125 °C temperature range for Racyics ABX aware timing and power sign-off
- Full statistical LVF characterization for low voltage operation



DESIGN VIEWS

- Verilog simulation models
- .lib /.db timing (NLDM, CCS, LVF) and power models
- .lef layout abstract views
- GDSII layouts
- LVS netlist

IP SPECIFICATION

IP	Supplier	Description	Supply Voltages [V]	ZBB (Zero Bias)	ABB	Ready for Evaluation	Ready for Testchip	Ready for Production
ri_sram_gf22fdx_RS	Racyics	Single Rail SP SRAM generator for ULV designs	0.55 / 0.65 / 0.80	no	yes, RBB	now	now	now

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