Racyics® Universal Chiplet Interconnect Express PHY IP

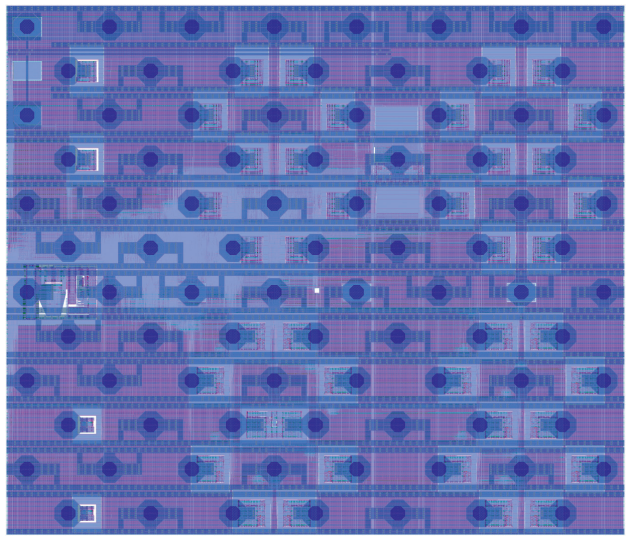
GlobalFoundries® 22FDX®

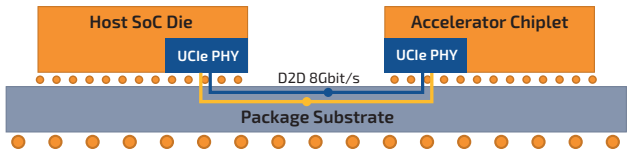
DESCRIPTION

The **Racyics UCIe PHY** is an energy-efficient chiplet interconnect IP solution for consumer and automotive applications. Implemented in **22FDX** technology, it supports 4 GT/s and 8 GT/s data rates while minimizing power consumption. The PHY is compliant with Automotive Grade 1 mission profiles and qualified on PDK-22FDX-PLUS-AutoPro150, ensuring reliable low-power operation in demanding automotive environments.

KEY FACTS

- Delivered as Hardmacro IP
- Implementation of the physical layer of the UCIe standard from Raw D2D Interface (RDI) to electrical interface of UCIe main band (MB) and sideband (SB)
- Includes TX and RX side
- Support for UCIe-S (standard package) configuration with x16 data width
- Data rates of 8 Gbit/s per pin and 4 Gbit/s per pin with half-rate clocking
- Integrated PLL for clock generation
- Integrated configuration and status register file with APB port
- Integrated link training and resistance calibration
- Automotive grade-1 reliability profile compliance with characterization corners from -40°C to 150°C
- 130 µm bump pitch
- Layout size 1143 x 1327.5 µm² (north/south chip edge)





DESIGN VIEWS

- Datasheet with integration guidelines
- Verilog simulation models
- GDSII layout
- LEF abstract
- .lib/.db timing models
- LVS netlist
- EMIR analysis models

IP SPECIFICATION

IP	Supplier	Description	Supply Voltage [V]	ZBB	ABB	Ready for Evaluation	Ready for Testchip	Ready for Production
ri_uciephy_gf22fdx	Racyics	UCIe PHY IP with X16 data width for standard package and up to 8 Gbit/s per pin data rate	0.80	yes	no	now	now	now

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