Ultra-low voltage logic designs using adaptive body biasing demand dense SRAM solutions which fully integrate in the adaptive body biasing aware implementation and sign-off flow of the Racyics® ABX Platform solution. The Racyics® Dual Rail SRAM supports ultra-low voltage core logic operation down to 0.4 V while operating dense, low leakage standard bit cells from a 0.8 V memory supply.

**KEY FACTS**

- Single port SRAM compiler based on P124 bitcell with Dual-supply-rail architecture
- Bitcell array supply voltage 0.8 V and ULV core interface down to 0.4 V enabled with Racyics® ABX
- Direct interfacing to ULV Racyics® ABX digital standard cell domains without additional level shifters
- Full set of characterization corners for -40 °C to 125 °C temperature range for Racyics® ABX aware timing and power sign-off
- Full statistical LVF characterization for low voltage operation
- Production test methodology available for adaptive body biasing

**DESIGN VIEWS**

- Verilog simulation models
- .lib/.db timing (NLDM, CCS, LVF) and power models
- .lef layout abstract views
- Milkyway database
- GDSII layouts
- LVS netlist

**IP SPECIFICATION**

<table>
<thead>
<tr>
<th>IP</th>
<th>Supplier</th>
<th>Description</th>
<th>Supply Voltages [V]</th>
<th>ZBB (Zero Bias)</th>
<th>ABX</th>
<th>Ready for Evaluation</th>
<th>Ready for Testchip</th>
<th>Ready for Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>rm_gf22fdx_1p</td>
<td>Racyics</td>
<td>Dual-Rail SP SRAM generator for ULV designs</td>
<td>core logic: 0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 bitcells: 0.80V</td>
<td>yes</td>
<td>yes, FBB</td>
<td>now</td>
<td>now</td>
<td>now</td>
</tr>
</tbody>
</table>