The Racyics® ABX Generator IP is a body bias voltage generator for the Racyics® ABX Platform for GLOBALFOUNDRIES 22FDX® technology. It contains a closed loop body bias regulation loop to generate N-well and P-well bias voltages for adaptive compensation of process, voltage and temperature (PVT) variations during device operation.

**KEY FACTS**

- Integrated adaptive body bias control loop
- Charge pumps for N-Well and P-Well voltages, operated from IO supply voltage level, reverse bias capability
- Integrated PVT monitors
- Independent regulation of NMOS and PMOS performance
- Operation from typically 10 MHz reference clock, optionally use of Racyics ULP 10 MHz Clock Generator to run from clocks down to 32 kHz
- Supports forward (FBB) and reverse body bias (RBB)
- Available in multiple charge pump drive strengths supporting a wide range of active chip areas
- Delivered as hardmacro for seamless integration
- Power consumption <10 µW

**DESIGN VIEWS**

- Verilog simulation models
- .lib/.db timing and power models
- .lef layout abstract views
- Milkyway database
- GDSII layout
- LVS netlist

**RACYICS® ABX VPW AND VNW ADAPTION**

**IP SPECIFICATION**

<table>
<thead>
<tr>
<th>IP Type</th>
<th>Supplier</th>
<th>Specification</th>
<th>Supply Voltages [V]</th>
<th>Ready for Evaluation</th>
<th>Ready for Testchip</th>
<th>Ready for Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABX controller IP hardmacro</td>
<td>Racyics</td>
<td>$f_{ref}=10$ MHz $P_{act}&lt;10$ µW Area &lt;0.0062 mm² -0.2V&lt;VNW&lt;2.4V -2.4V&lt;VPW&lt;0.2V Body bias generation: 1.80V Control logic: 0.80V PVT monitors: 0.40V/0.45V/0.50V/0.60V/0.65V/0.80V/0.90V</td>
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