Body biasing is a disruptive 22FDX® feature enabling on-the-fly adaption of transistor threshold voltages. Racyics® adaptive body biasing platform (Racyics® ABX Platform) provides reliable and predictable ultra-low voltage (ULV) operation down to 0.4V, compensating process, supply voltage and temperature variations (PVT) to guarantee timing and power with high yield.

**KEY FACTS**
- Comprehensive Racyics® ABX Platform for ULV operation
- Racyics® adaptive body bias generator, standard cells, SRAM
- Up to 9X performance
- 75% leakage reduction
- Corner tightening and adaptive body biasing-aware implementation for improved PPA
- Guaranteed performance and power
- Easy-to-use turnkey Racyics® ABX solution based on standard design flow and sign-off
- No overhead in test and operation

**TARGET APPLICATION**
- Automotive
- Low Power
- IoT
- High Speed Computing

**IP OFFERING**

<table>
<thead>
<tr>
<th>IP Type</th>
<th>Supplier</th>
<th>Description</th>
<th>Ready for Evaluation</th>
<th>Ready for Testchip</th>
<th>Ready for Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Cells incl. PMK</td>
<td>Racyics</td>
<td>104CPP 9T CNRX STD-cell library, fully ABX enabled (FBB, RBB), supply voltages 0.40V/0.45V/0.50V/0.60V/0.80V</td>
<td>now</td>
<td>now</td>
<td>now</td>
</tr>
<tr>
<td>Standard Cells incl. PMK</td>
<td>Racyics</td>
<td>116CPP 8T CNRX STD-cell library, fully ABX enabled (FBB, RBB), supply 0.40V/0.45V/0.50V/0.60V/0.80V</td>
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<td>now</td>
<td>now</td>
</tr>
<tr>
<td>SRAM</td>
<td>Racyics</td>
<td>Dual-Rail SP SRAM generator for ULV designs, supply 0.40V/0.45V/0.50V/0.60V/0.80V (core) 0.80V (bitcells)</td>
<td>now</td>
<td>now</td>
<td>now</td>
</tr>
<tr>
<td>ABX Generator IP</td>
<td>Racyics</td>
<td>Racyics® ABB generator, includes PVT monitors, bias generator, digital control loop, supports FBB and RBB</td>
<td>now</td>
<td>now</td>
<td>now</td>
</tr>
</tbody>
</table>

**EXAMPLE ULV SOC WITH RACYICS® ABX IP**

- ULL logic (0.8V)
- Analog (0.8V)
- Interfaces (1.8V/0.8V)
- ULV logic (0.4V ... 0.6V)
- ULV SRAM (Dual Rail 0.4V...0.6V, 0.8V)
- ABB domain
- ABB Generator IP
- PVT monitors
- BBGEN (VNW, VPW)
- ADPLL controller

**PLATFORM KIT**

- Standard Cells incl. PMK
- Dual Rail SRAM
- ABX Generator IP
- IO Library
- Clock Generation (ADPLL)