The general purpose 22FDX® IO Library features a rich set of digital and analog IO cells covering 1.2 V to 1.8 V I/O standards and 0.4 V to 0.8 V core voltages. Diverse special function cells are included. There is no need for specific back-biasing. Full bulk isolation and various bond options are available.

### KEY FACTS
- Library contains approx. 60 IO cells
- Support for all metal-stacks of 22FDX®
- Low voltage cells with nominal core voltages down to 0.4 V for glue-less interfacing to ULV Racyics® ABX digital standard cell domains
- Low leakage cells for ultra low power always-on domain usage
- Highly configurable dual-GPIO cells with LVDS transceiver mode
- High-speed multi-standard differential IO cell supporting LVDS, SGMII, SATA, PCIe, PECL, CML, with AC and DC coupling and digitally calibrated termination
- Power-on-reset cell
- Analog IOs, calibrated reference voltage

### DESIGN VIEWS
- Verilog simulation models
- .lib/.db timing and power models (NLDM)
- IBIS models
- .lef layout abstract views
- Milkyway database
- GDSII layouts
- LVS netlist

### IP SPECIFICATION

<table>
<thead>
<tr>
<th>IP</th>
<th>Supplier</th>
<th>Description</th>
<th>Supply Voltages [V]</th>
<th>ZBB (Zero Bias)</th>
<th>ABX</th>
<th>Ready for Evaluation</th>
<th>Ready for Testchip</th>
<th>Ready for Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>rilib_g22fdx_io_GoodpastoralV</td>
<td>Racyics</td>
<td>General purpose IO combined GPIO/LVDS high-speed multi-standard differential IO Analog and Special Functions</td>
<td>1.2/1.5/1.8 core: 0.40/ 0.45/ 0.50/ 0.60/ 0.65/ 0.80 (cell-type dependent)</td>
<td>yes</td>
<td>no</td>
<td>now</td>
<td>now</td>
<td>now</td>
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</tbody>
</table>