Racyics® ULP 10MHz Clock Generator
GLOBALFOUNDRIES® 22FDX®

DESCRIPTION

Ultra-low power 10 MHz clock multiplier from a low frequency reference

APPLICATION

The Racyics® clock generator is designed to generate a 10 MHz clock from a low-frequency reference with as little power and area overhead as possible. For highest flexibility, a wide range of reference frequencies is supported. The generated clock can be fed to the Racyics® ABX generator.

KEY FACTS

- The All Digital Frequency Locked Loop (ADFLL) architecture is reduced to the minimum amount of hardware necessary to generate a 10 MHz clock
- High energy efficiency: Only 5 µW are consumed during operation
- A reference clock divider allows reference clock frequencies from 32 kHz to 1 MHz

DESIGN VIEWS

- Verilog simulation models
- .lib/.db timing and power models (NLDM)
- .lef layout abstract views
- Milkyway database
- GDSII layouts
- LVS netlist

IP SPECIFICATION

<table>
<thead>
<tr>
<th>IP</th>
<th>Supplier</th>
<th>Description</th>
<th>Supply Voltages [V]</th>
<th>ZBB (Zero Bias)</th>
<th>ABX</th>
<th>Ready for Evaluation</th>
<th>Ready for Testchip</th>
<th>Ready for Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>ri_gf22fdx_clkgen_10m</td>
<td>Racyics</td>
<td>ULP 10 MHz Clock-Generator</td>
<td>0.80</td>
<td>yes</td>
<td>no</td>
<td>now</td>
<td>now</td>
<td>now</td>
</tr>
</tbody>
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