Racyics® ULV Clock Generator
GLOBALFOUNDRIES® 22FDX®

DESCRIPTION

Adaptive body bias-enabled, All-Digital PLL clock generator for ultra-low power clocking in highly energy efficient Systems on Chips

APPLICATION

The Racyics® Ultra-Low Voltage Clock Generator is targeted at Systems on Chip (SoCs) employing advanced power management techniques. The robust, fully digital architecture allows operation in a wide voltage and frequency range. Unique fast lock and instant frequency change features maximize the energy efficiency of the targeted systems.

KEY FACTS

- The fully digital architecture allows operation from 0.4 to 0.8 V and from 20 MHz up to 1 GHz.
- Very energy efficient, especially at low supply voltages: Only 100 µW power consumption for a 100 MHz output clock at 0.5V
- A custom DCO allows fast lock-in and instant frequency changes during operation through direct tuning value calculation and without additional hardware
- The Racyics® ABX enabled implementation reduces jitter at low supply voltages

DESIGN VIEWS

- Verilog simulation models
- .lib/.db timing and power models (NLDM)
- .lef layout abstract views
- Milkyway database
- GDSII layouts
- LVS netlist

IP SPECIFICATION

<table>
<thead>
<tr>
<th>IP</th>
<th>Supplier</th>
<th>Description</th>
<th>Supply Voltages [V]</th>
<th>ZBB (Zero Bias)</th>
<th>ABX</th>
<th>Ready for Evaluation</th>
<th>Ready for Testchip</th>
<th>Ready for Production</th>
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<tbody>
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<td>ri_gf22fdx_clkgen</td>
<td>Racyics</td>
<td>ULV Clock-Generator</td>
<td>0.40/ 0.45/ 0.50/ 0.60/ 0.65/ 0.80</td>
<td>yes</td>
<td>yes, FBB</td>
<td>now</td>
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