

Racyics® ULP 10MHz Clock Generator

GLOBALFOUNDRIES® 22FDX®



DESCRIPTION

Ultra-low power 10 MHz clock multiplier from a low frequency reference.

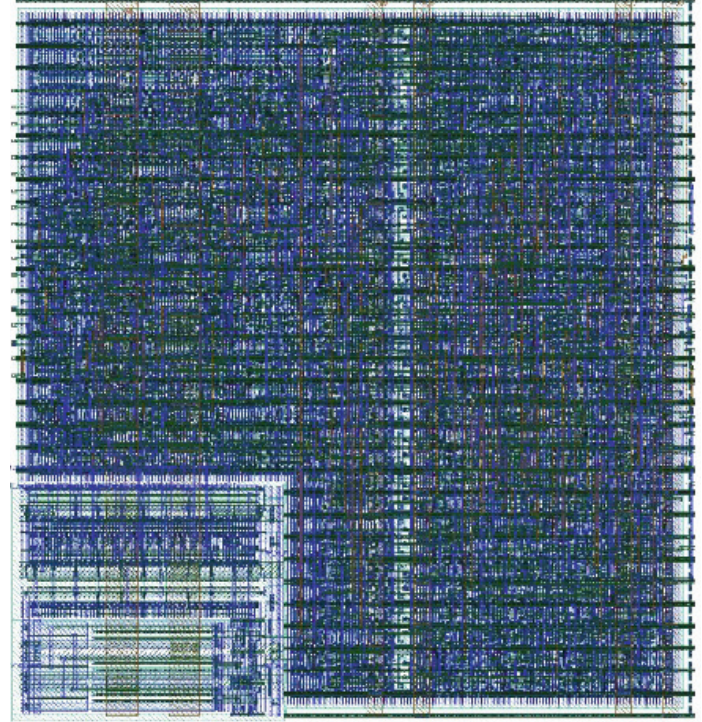
APPLICATION

The **Racyics®** clock generator is designed to generate a 10 MHz clock from a low-frequency reference with as little power and area overhead as possible.

For highest flexibility, a wide range of reference frequencies is supported. The generated clock can be fed to the **Racyics® ABX®** generator.

KEY FACTS

- ▶ The All Digital Frequency Locked Loop (ADPLL) architecture is reduced to the minimum amount of hardware necessary to generate a 10 MHz clock
- ▶ High energy efficiency: Only 5 μ W are consumed during operation
- ▶ A reference clock divider allows reference clock frequencies from 32 kHz to 1 MHz



DESIGN VIEWS

- ▶ Verilog simulation models
- ▶ .lib /.db timing and power models (NLDM)
- ▶ .lef layout abstract views
- ▶ NDM and Milkyway libraries
- ▶ GDSII layouts
- ▶ LVS netlist

IP SPECIFICATION

IP	Supplier	Description	Supply Voltages [V]	ZBB (Zero Bias)	ABB	Ready for Evaluation	Ready for Testchip	Ready for Production
ri_gf22fdx_clkgen_10m	Racyics®	ULP 10 MHz Clock Generator	0.80	yes	no	now	now	now



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