Racyics® IP Catalog 2025

GLOBALFOUNDRIES® 22FDX®

Racyics® provides IP Products for GlobalFoundries® 22FDX®, enabling ultra-low-power, high-performance system-on-chip (SoC) designs. With a focus on adaptive body biasing (ABB), efficient power management, and robust clock generation, our IP portfolio ensures optimal performance and energy efficiency across a wide range of applications.

	IP	Key Features			Technology GF® 22FDX® EXT	Technology GF® 22FDX® PLUS
ABX	Racyics® **Adaptive Body Bias (ABB)** Generator IP for GF® 22FDX® (ABX)	**Supply:** Body bias generation: **1.80 V** Control logic: **0.80 V** Integrated **ABB control loop** fref = < **10 MHz to 50 MHz** > area < 0.006 mm² (smallest pump strength) Independent Adaption: **-0.2 V < VNW < 2.4 V** **-2.4 V < VPW < 0.2 V**				
ABX	• consumer	PVT monitors: 0.40 V / 0.45 V / 0.50 V / 0.55 V / 0.65 V / 0.80 V / 0.90 V Pactive < **12 µW** (typical)			✓	✓
ABX	• automotive	PVT monitors: 0.80 V Pactive < **200 µW** (typical) **Automotive grade-1 and grade-2** compliant ISO26262 SEooC with **ASIL D** capability			✓	***
ABX	Racyics® **Standard Cell Libraries** with > 300 cells	**Supply:**	**VT Options:**	**Gate Length:**		
ABX	• **8T**	0.40 / 0.45 / 0.50 / 0.60 / 0.80 V ABB: **forward body bias**	SLVT, LVT	C20, C24, C28, C32, C36	✓	*
ABX	• **8T**	0.55 / 0.80 / 0.90 V ABB: **reverse body bias**	RVT, HVT	C20, C24, C28, C32, C36	✓	*
ABX	• **9T** automotive grade 1	0.80 V ABB: **reverse body bias**	RVT, HVT	C20, C24, C28, C32, C36	✓	(✓)*
ABX		Characterization corners for - 40 °C to 150 °C temperature range for **Racyics® ABX aware timing and power sign-off**				
ABX PLATFORM	**Dual-Rail Single Port SRAM** generator for ULV designs with forward body bias capability	**Supply:** core logic: 0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 V bitcells: 0.80 V ABB: **forward body bias**	6t SRAM based on P124 bitcell Power saving mode: **retention mode** & option to reduce VDD supply during inactivity		✓	*
ABX PLATFORM	**Single-Rail Single Port SRAM** generator for ULV designs with reverse body bias capability	0.55 / 0.80 V ABB: **reverse body bias**	6t SRAM based on R188 bitcell Power saving mode: option to reduce VDD supply during inactivity		✓	*
ABX PLATFORM	**Single-Rail Single Port SRAM** with Power Down with reverse body bias capability	0.55 / 0.80V ABB: **reverse body bias**	6t SRAM based on R188 bitcell Power saving mode: **retention mode & power down**		✓	*
ABX PLATFORM	**Single-Rail Single Port ROM** (read-only memory) Macros	0.55 / 0.80 (0.65) V ABB: **reverse body bias**	option to reduce VDD supply during inactivity		✓	*
ABX PLATFORM	**Single-Rail Single Port cryo-optimized SRAM** (Static Random Access Memory) with Power Down	0.80 V ABB: **forward body bias*** **	6t SRAM based on S188 bitcell **Prototype optimized for Cryo** Power saving mode: **retention mode & power down**		✓***	*
ABX PLATFORM	**Micro Two Port, Dual-Rail, forward-bias SRAM** (Static Random Access Memory)	0.8 V ABB: **forward body bias**	**8t SRAM based on R250 bitcell**		✓***	*

* Available for GF® 22FDX® PLUS up on request.
** IP is ready for production in Q2/2025.
*** Currently in development.

Racyics® IP Catalog 2025

GLOBALFOUNDRIES® 22FDX®

	IP	Key Features		Technology GF® 22FDX® EXT	Technology GF® 22FDX® PLUS
ULP PLATFORM	Racyics® **Digital Wrapper for Clock and Power Supply IP** for GF® 22FDX®	**Supply:**		✓	*
	• **Low Power Bandgap** Voltage Reference	VDDA18: 1.62 V - 1.98 V VDD: 0.72 V - 0.88 V	two separate output voltages: **400 mV** and **600 mV** with independent trimming, reference-good detection signal	✓	*
	• nominal **50 MHz Frequency Clock Generator**	0.8 V (Vref= 0.6 V)	**< 50 ps RMS period jitter** and < 800 ps total jitter (TJ) < 5 ps / mV supply sensitivity power consumption **10 uW** typical and 30 uW maximum	✓	*
	• step-down **DC-to-DC Voltage Converter** (Buck Converter)	VDDA18, VDDP 18:1.62 - 1.98 V VDD: 0.72-0.88 V	Output voltage **0.4 V - 0.9 V** in steps of 25 mV can be software-configured on-the-fly enables Dynamic Voltage and Frequency Scaling **can power ABX domain**	✓	*
	• **Linear Regulator** 1.8 V to core supply	1.8 V (Vref= 0.4V)	1.8 V input to 0.8 V output Output current up to 8 mA Power good indication **disable function** for low power consumption < **0.5 uW**	✓	*
RACYICS COMPLEMENTARY IP PRODUCTS	General purpose **1.8 V IO Library** with combined GPIO / LVDS, Analog and Special Function IOs	**Supply:** IO: 1.2 / 1.5 / 1.8 core: 0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 (cell-type dependent)	supports a wide range of **Metalstack Options** Various **Pads & Bump** Sizes ~ 60 IO cells	✓	*
	All-Digital Phase Lock Loop (ADPLL) **2 GHz Clock Generator** based on a Digitally Controlled Oscillator (DCO) with programmable clock frequency dividers	0.80	800 MHz < = **DCO frequency** < = 2400 MHz **lock-in < 25 us** **8-phase** clock output (each 45° phase shift) Compliant to automotive grade-1 fref up to 150 MHz < 15 ps RMS longterm jitter	✓	*
	ULP All Digital Frequency Locked Loop (ADFLL) **10 MHz Clock Generator**	0.80	**10 MHz clock** **High energy efficiency: 5 µW** during operation fref = < 32 kHz to 1 MHz> Can be used as clock input for Racyics® ABX generator	✓	*
	ULV Integer-N Bang-Bang All-Digital Phase Locked Loop (BB-ADPLL) **1 GHz Clock Generator** In a fully digital architecture	0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 V	**20 MHz up to 1 GHz**. **100 uW power consumption** for a 100 MHz output clock at 0.5 V fast lock-in and instant frequency changes The Racyics® ABX enabled implementation reduces jitter at low supply voltages.	✓	*
	Voltage and Temperature Sensor with integrated analog-to-digital converter (ADC) and band-gap voltage reference	VDDA 1.62 V to 1.98 V VDD 0.8 V	3 single-ended voltage measurement inputs **1st order Delta-Sigma ADC** with configurable oversampling ratio Resolution up to 12 bit	✓**	*
	crystal oscillator designed to work with 32 kHz crystal	IO: 1.8 V core : 0.8 V	Bypass & Off mode, t_startup ~ 58 ms compatible with Racyics IO lib	✓**	*

* Available for GF® 22FDX® PLUS up on request.
** IP is ready for production in Q2/2025.
*** Currently in development.