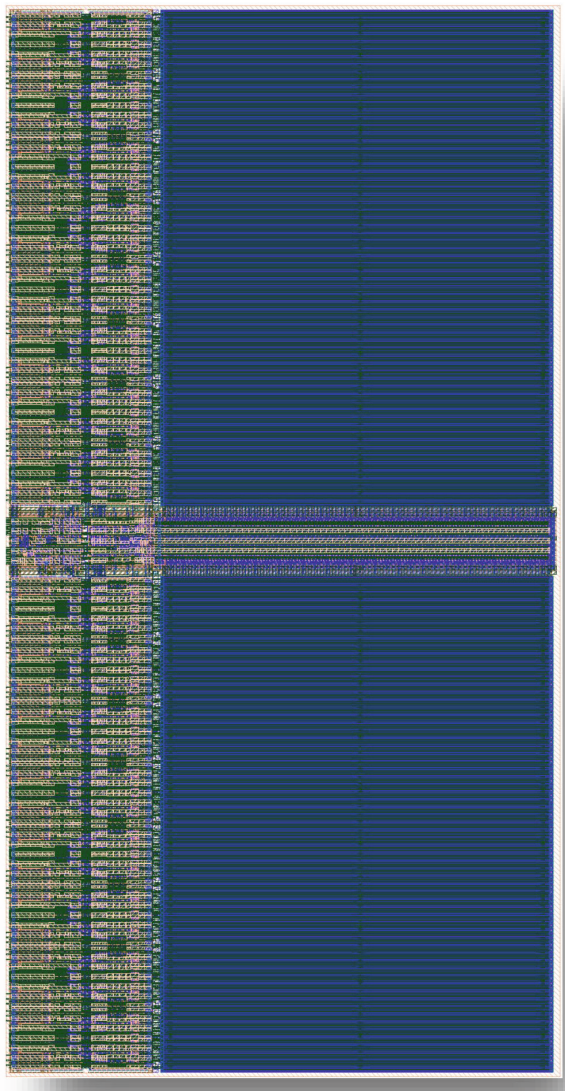
Racyics® Dual Rail SRAM

GLOBALFOUNDRIES® 22FDX®

CHALLENGE

Ultra-low voltage logic designs using adaptive body biasing demand dense SRAM solutions which fully integrate in the ABB aware implementation and sign-off flow of the **Racyics® ABX® Platform** solution. The **Racyics®** Dual Rail SRAM supports ultra-low voltage core logic operation down to **0.4 V** while operating dense, low leakage standard bit cells from a 0.8 V memory supply.



KEY FACTS

- Single port SRAM compiler based on P124 bitcell with Dual-supply-rail architecture
- Bitcell array supply voltage 0.8 V and ULV core interface down to 0.4 V enabled with **Racyics®** ABB
- Power saving modes available when SRAM not in use
- Direct interfacing to ULV **Racyics® ABX®** digital standard cell domains without additional level shifters
- Full set of characterization corners for -40 °C to 125 °C temperature range for **Racyics® ABX®** aware timing and power sign-off
- Full statistical LVF characterization for low voltage operation
- Production test methodology available for ABB

DESIGN VIEWS

- Verilog simulation models
- .lib /.db timing (NLDM, CCS, LVF) and power models
- .lef layout abstract views
- NDM and Milkyway libraries
- GDSII layouts
- LVS netlist

IP SPECIFICATION

IP	Supplier	Description	Supply Voltages [V]	ZBB (Zero Bias)	ABB	Ready for Evaluation	Ready for Testchip	Ready for Production
ri_sram_gf22fdx_LL	Racyics®	Dual-Rail SP SRAM generator for ULV designs	core logic: 0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 bitcells: 0.80	yes	yes, FBB	now	now	now

Racyics GmbH

Main Office
Bergstraße 56
01069 Dresden
Germany

Duisburg Office
Schifferstraße 196
47059 Duisburg
Germany

Frankfurt Office
Siemensstraße 10a
63263 Neu-Isenburg
Germany