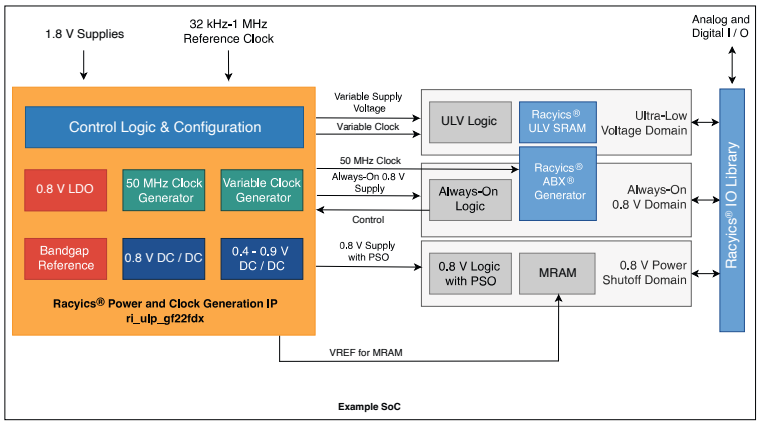
Racyics® Power and Clock Generation IP

GLOBALFOUNDRIES® 22FDX®

DESCRIPTION

Tightly integrated power management platform with a soft-IP wrapper around Analog / Mixed-Signal hard macros which generate all supply voltages and clock signals needed to run highly efficient SoCs in **GlobalFoundries® 22FDX®**. Running from only one supply voltage and reference clock, the IP generates its own internal supplies and references, and those needed to run the **Racyics® ABX®** Generator. With a simple digital interface, and a comprehensive register file for configuration, the IP simplifies chip power management and can be customized to a wide range of applications.

INTEGRATION EXAMPLE



Supply and Reference Voltages

- 0.8 V supplies for always-on logic and a power-shutoff domain
- Seamless switching between LDO and DC / DC converter for fast startup and high efficiency
- Variable 0.4 to 0.9 V supply for additional power domains supporting up to 250 mA load current
- 0.6 V voltage reference for MRAM

Clock Generation

- Ultra-low power 50 MHz clock generator
- Variable-frequency PLL clock generator with a wide frequency range reaching up to 500 MHz

Control Logic

- Simple handshake protocol for selecting IP operation modes with different power and clock generation settings
- APB interface and explicit inputs for detailed configuration of each sub-block
- Reference clock failure detection and handling for safe shutdown of high-current circuits

DESIGN VIEWS

- APL views for EMIR analysis
- Datasheet with integration guidelines
- GDSII layout
- LEF abstract
- .lib / .db timing
- LVS netlist
- Verilog simulation models
- Synthesizable controller RTL with implementation constraints

IP SPECIFICATION

IP	Description	Power typ. 25° C / max. 125° C	Area
ri_bgr_gf22fdx_ulp	Voltage reference with buffered 0.6 V reference for MRAM and 0.4 V and 0.6 V references for power and clock generation	30 / 43 uW without buffer 59 / 84 uW with buffer enabled	165 x 95 um
ri_ldo_gf22fdx	LDO regulator for generating 0.8 V from 1.8 V for fast start-up	10 nW / 1 uW disabled 38 / 62 uW enabled	50 x 60 um
ri_dcdc_gf22fdx_buck	DC / DC converter for generating 0.4-0.9 V from 1.8 V	up to 95 % conversion efficiency < 3 uW / < 30 uW disabled 36 uW / 85 uW enabled	180 x 80 um
ri_clkgen_gf22fdx_50m	Ultra-low power 50 MHz FLL clock generator	1 / 20 uW disabled 10 / 30 uW enabled	50 x 40 um
ri_adpll_gf22fdx_500m	200 to 500 MHz PLL clock generator	75 / 170 uW at 200 MHz running from 10 MHz 125 / 240 uW at 500 MHz running from 10 MHz	60 x 70 um
ri_ulp_gf22fdx	Digital soft-IP wrapper for IP control and configuration with APB interface and register file		10 000 NAND gate equivalents

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