

# Racyics® ADPLL 2GHz Clock Generator

GlobalFoundries® 22FDX®

Racyics

## DESCRIPTION

All-digital phase locked loop (ADPLL) clock generator for a nominal frequency of 2 GHz (0.8 V).

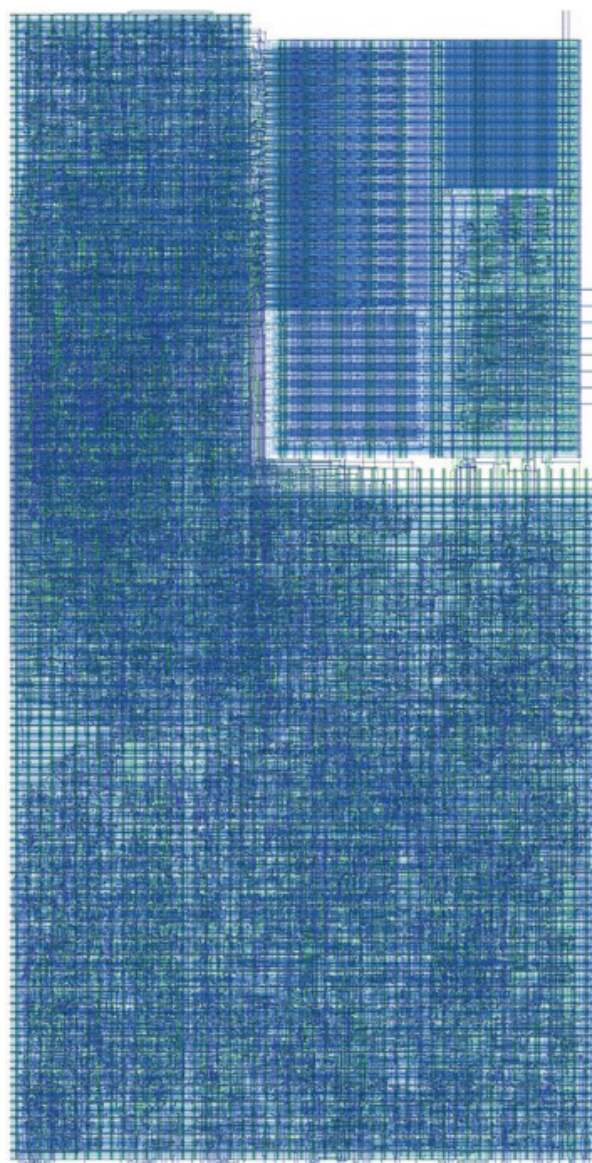
## Application

The Racyics all-digital phase locked loop (ADPLL) clock generator is designed to generate a nominal 2 GHz multi-phase clock from a low-frequency reference with as little power and area overhead as possible.

For highest flexibility, a wide range of reference frequencies for the Digitally Controlled Oscillator (DCO) is supported.

## KEY FACTS

- ▶ Clock generation based on a Digitally Controlled Oscillator (DCO)
- ▶  $800 \text{ MHz} \leq \text{DCO frequency} \leq 2400 \text{ MHz}$
- ▶ Programmable clock frequency dividers for ADPLL loop and clock outputs
- ▶ lock-in  $< 25 \mu\text{s}$
- ▶ 8-phase clock output (each  $45^\circ$  phase shift)
- ▶ Compliant to automotive grade-1
- ▶ allows reference frequency up to 150 MHz
- ▶  $< 15 \text{ ps RMS}$  longterm jitter (measured over 1 ms)
- ▶ Characterization corners for  $-40^\circ\text{C}$  to  $150^\circ\text{C}$



## DESIGN VIEWS

- ▶ Verilog simulation models
- ▶ .lib / .db timing and power models (NLDM)
- ▶ .lef layout abstract views
- ▶ GDSII layouts
- ▶ LVS netlist

## IP SPECIFICATION

IP	Supplier	Description	Supply Voltages [V]	ZBB (Zero Bias)	ABB	Ready for Evaluation	Ready for Testchip	Ready for Production
ri_adpll_gf22fdx_2gmp	Racyics	ADPLL 2GHz Clock Generator	0.80	yes	no	now	now	now



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