

Racyics® ULV Clock Generator

GlobalFoundries® 22FDX®

Racyics

DESCRIPTION

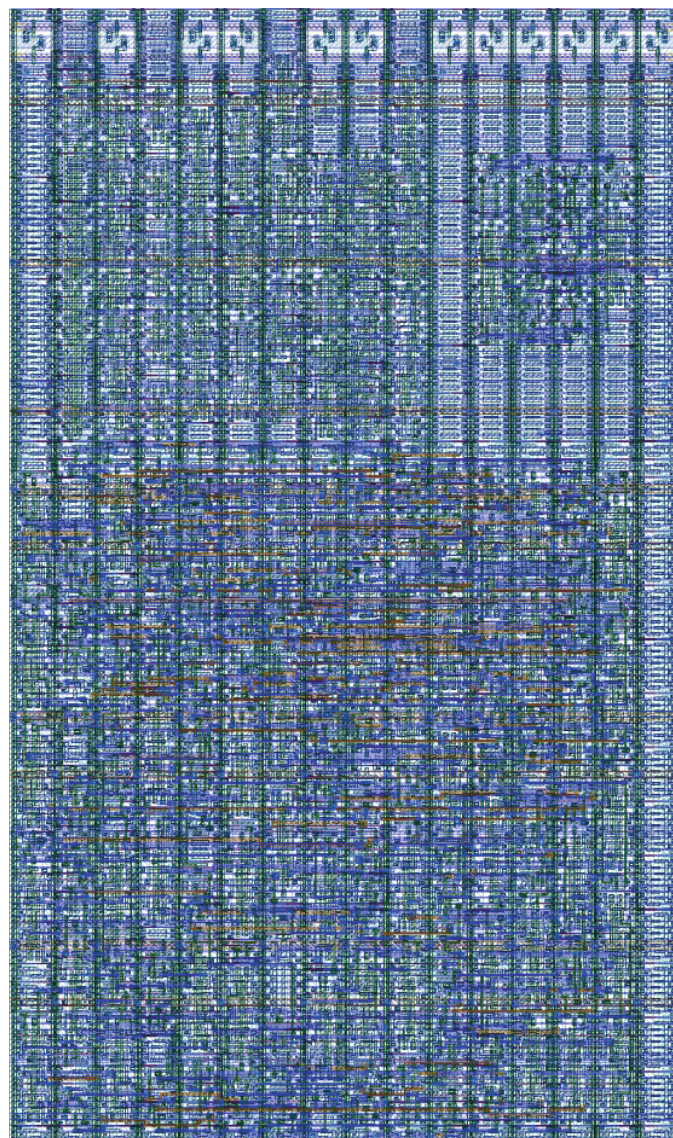
ABB-enabled, All-Digital PLL clock generator for ultra-low power clocking in highly energy efficient Systems on Chip.

APPLICATION

The Racyics Ultra-Low Voltage Clock Generator is targeted at Systems on Chip (SoCs) employing advanced power management techniques. The robust, fully digital architecture allows operation in a wide voltage and frequency range. Unique fast lock and instant frequency change features maximize the energy efficiency of the targeted systems.

KEY FACTS

- ▶ The fully digital architecture allows operation from 0.4 to 0.8 V and from 20 MHz up to 1 GHz.
- ▶ Very energy efficient, especially at low supply voltages: Only 100 μ W power consumption for a 100 MHz output clock at 0.5 V.
- ▶ A custom DCO allows fast lock-in and instant frequency changes during operation through direct tuning value calculation and without additional hardware.
- ▶ The **Racyics ABX®** enabled implementation reduces jitter at low supply voltages.



DESIGN VIEWS

- ▶ Verilog simulation models
- ▶ .lib / .db timing and power models (NLDM)
- ▶ .lef layout abstract views
- ▶ GDSII layouts
- ▶ LVS netlist

IP SPECIFICATION

| IP | Supplier | Description | Supply Voltages [V] | ZBB (Zero Bias) | ABB | Ready for Evaluation | Ready for Testchip | Ready for Production |
|-------------------|----------|---------------------|---|-----------------|----------|----------------------|--------------------|----------------------|
| ri_gf22fdx_clkgen | Racyics | ULV Clock Generator | 0.40 / 0.45 / 0.50 / 0.60 / 0.65 / 0.80 | yes | yes, FBB | now | now | now |



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